FAIRCHILD
SEMICONDUCTOR®

AN5400
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- Eight 13-Bit DACs on the SPT5400
- Voltage Output to a Maximum of ±4.5 V on Each DAC
- On-Board Address, Load and Write Circuits
- SMA Connectors on the DAC Outputs
- Two Clock Input Connections
- On-Board Manual Chip Select and Clear
- On-Board Reference Circuit
- Automatic or Manual Control of DAC Registers
- Prototype Area for Analog and Digital Circuitry

APPLICATIONS

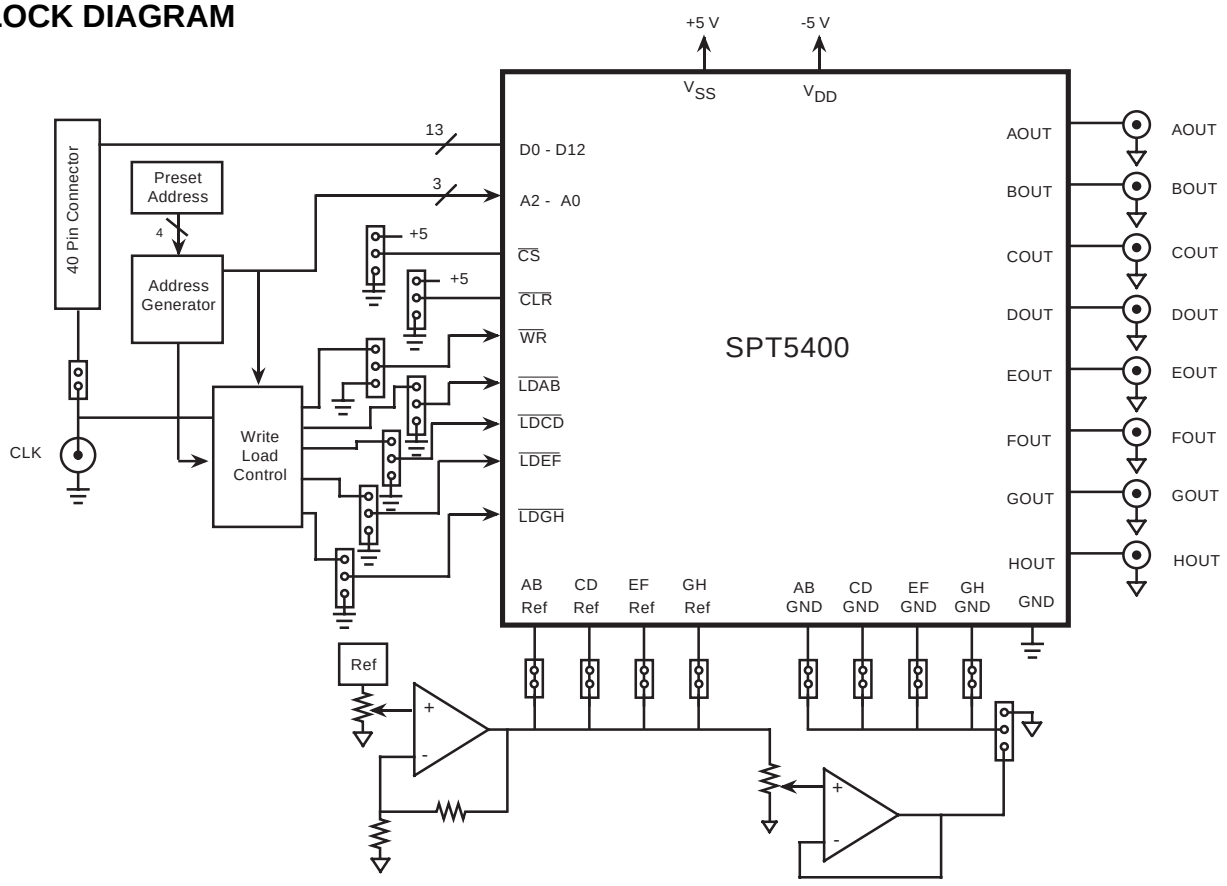
- Evaluation of the SPT5400 DAC
- Eight Analog Controls as Subsystem
- 13-Bit Precision Control System
- Engineering Prototype Aid
- Guide to PCB Layout
- Guide for Design of SPT5400

GENERAL DESCRIPTION

The SPT5400 is a 13-bit octal DAC capable of outputting bipolar values of up to ±4.5 V with a supply voltage of ±5 V. There are two separate reference input pins (Reference High and Analog Ground pin) for each DAC pair. (DAC pairs are delineated as AB, CD, EF and GH respectively.) As many as four separate reference inputs are available for all eight DACs. It is possible to produce four different full-scale output voltages with a resolution of 13 bits (full scale/8192) from the four DAC pairs. The SPT5400 is capable of bipolar, unipolar (positive or negative) or custom output voltages. The voltage output of each DAC is a single-ended source. The SPT5400 provides for a double latch of the data or may be set to transparent mode for each DAC. An asynchronous clear (/CLR) pin clears the data value in the DAC to a 1000H bit pattern for a mid scale voltage output.

This device is ESD sensitive. All ESD precautions should be exercised when handling this device.

BLOCK DIAGRAM



The EB5400 evaluation board is a tool for device evaluation and characterization and demonstrates the performance of the SPT5400 (13-bit, octal DAC). The SPT5400 accepts up to 13 binary bits into its logic inputs. The clock signal source may be provided from one of two input sources, the logic connector or an SMA connector.

Various termination schemes are provided, depending on the type of clock signal used. The data is presented to the SPT5400, then, depending on the control lines of the address (load and write), the data is transferred to the selected DAC. The output voltage is a function of the reference voltages (see the Reference section) at the Reference High and AGND pins for the selected DAC.

This application note is a supplement to the data sheet and includes more detailed technical information on the interfacing circuits required to operate the SPT5400. The evaluation board is designed to accommodate a wide variety of applications and can be easily modified to suit a specific application with the use of the prototype area provided. Contact the Fairchild Applications Engineering Department if assistance is needed.

This application note describes in more detail the functional blocks of the evaluation board. The topics include Power Supplies and Grounding, Logic Interface Circuit, Conversion Clock, Analog Output, Reference Circuits and Layout.

POWER SUPPLIES AND GROUNDING

The EB5400 is powered by +5 V and -5 V supplies. The +D5 V supplies the digital control circuitry ('161 counter, '32 OR gates and '139 dual two-four decoder). You can feed it through a ferrite bead (FB2, socketed) and filter it to supply the analog +5 V (+A5 V) power plane. Alternately, the +A5 V may be the primary supply and you may feed the +D5 V back through the ferrite bead. Another option is use two separate +5 V supplies to supply the two +5 V when more isolation is required (remove FB2). The +A5 V is the supply for the analog section (+5 V, V_{DD} of the DAC and +5 V for the reference source and reference op amp). The -A5 V supply is used for the DAC's V_{SS} and the op amp's negative supply. Adequate isolation filtering and decoupling of the power between the analog and digital circuits have been incorporated into the design; however, Fairchild recommends that you use low-noise (nonswitching), regulated and low source impedance supplies. Refer to table I for power and signal connections.

Power is brought onto the evaluation board via the P1 connector or may be injected into the test point terminals as labeled. Power distribution to the analog +5 V of the SPT5400 is filtered to isolate it from the digital switching noise associated with the TTL signals. Fairchild recommendes that you use a similar design approach when using a single +5 V supply.

The power return connections and grounding are accomplished with a split ground plane: one for the digital return and one for the analog return. The two ground planes are coupled together through a ferrite bead (FB1) near the DAC. This reduces the high-speed digital switching signal noise from disturbing the low-noise analog section.

Power up should be done in the following sequence: V_{SS}, V_{DD}, references and, finally, the logic inputs. The power supply voltages should be at their nominal operating levels before applying digital logic signals to this device. If this sequence is not possible, limit the input voltage level at the logic input pins to no more than +0.3 V above V_{DD} during power up. Ensure that the absolute maximum voltage ratings are not exceeded at power up.

Table I - P1, Pinouts

Pin #	Description	Pin #	Description
1	Clock	2	Digital Ground
3	D0 (l LSB)	4	Digital Ground
5	D1	6	Digital Ground
7	D2	8	Digital Ground
9	D3	10	Digital Ground
11	D4	12	Digital Ground
13	D5	14	Digital Ground
15	D6	16	Digital Ground
17	D7	18	Digital Ground
19	D8	20	Digital Ground
21	D9	22	Digital Ground
23	D10	24	Digital Ground
25	D11	26	Digital Ground
27	D12	28	Digital Ground
29	NC	30	Digital Ground
31	+D5 V	32	Digital Ground
33	-A5 V	34	Analog Ground
35	-A5 V	36	Analog Ground
37	+A5 V	38	Analog Ground
39	+A5 V	40	Analog Ground

DATA INPUT

Negative transients at the data inputs or control pins should not be allowed. Note that there are 4.7 kΩ resistors in parallel with the data inputs. These reduce the transients for the data input. Ensure that the SPT5400 is powered up before any logic input is applied.

You can achieve simultaneous output voltage change by performing a write to each address and then simultanoeously providing a common load strobe to /LDAB, /LDCD, /LDEF and /LDGH to all DACs.

Asserting the clear pin (/CLR) will load 1000H (mid scale) into all of the latches in the DAC. Deasserting the chip select pin (/CS, high logic level) will force the outputs to stay at their last program level, provided that the /CLR signal has not been asserted.

CONTROL CIRCUITS

The SPT5400 DAC can be controlled by a combination of jumpers, digital control logic and analog reference voltages. The board can operate in many different modes and is easily modified to meet your DAC control needs. The value of the analog full-scale output voltage is a function of the set reference voltages. Refer to the Reference Voltage section for details on the output setting.

The following table outlines the control of jumpers, connectors, potentiometers and switches. Refer to the reference diagram to determine the location of each described name.

Table II - Control Table

NAME	DESCRIPTION
CLK (J2)	When jumpered, the clock source originates from the P1 connector. (Note: Typically remove the R14, 50 Ω termination resistor in this position.) The clock requires a TTL-level signal.
CLK (J3)	This is typically driven by a 50 Ω source. Ensure that R14 (50 Ω) is in and J2 is unjumpered. The clock requires a TTL-level signal.
J31	When jumpered to DGND, the clock source is enabled. When +5 V is jumpered, the clock is disabled.
/PE	When jumpered, the 161 counter's parallel load of the address select switch setting is enabled. This sets the address after at least one rising edge of clock.
Address Select	The switch setting selects the address of the DAC when the /PE is jumpered.
/LDAB	When jumpered to the auto position, the load signal to the DAC originates from control logic. In the fixed position, it forces the DAC input to be transparent for DACs A and B.
/LDCD	When jumpered to the auto position, the load signal to the DAC originates from control logic. In the fixed position, it forces the DAC input to be transparent for DACs C and D.
/LDEF	When jumpered to the auto position, the load signal to the DAC originates from control logic. In the fixed position, it forces the DAC input to be transparent for DACs E and F.
/LDGH	When jumpered to the auto position, the load signal to the DAC originates from control logic. In the fixed position, it forces the DAC input to be transparent for DACs G and H.
/WR	When jumpered to the auto position, the associated address determines which latch is loaded. In the fixed position, the A through H latches are transparent when the associated address is selected (both in conjunction with /CS).
/CS	This signal must be in the /CS position to allow the DAC latches to be loaded.
/CLR	This signal must be in the CLR position to allow the DACs to be loaded with values other than the fixed value of 1000H. In the /CLR position, it forces all DAC data inputs to 1000H, forcing the analog outputs to their mid scale level. (The value depends on the reference inputs.)
ABREF	When jumpered, it allows the value of the REF H (Reference High) voltage (from the on-board op amp) to be supplied to this reference input (high side). When unjumpered, an external high reference may be input to the pin closest to the DAC.
CDREF	Jumpering allows the value of the REF H (Reference High) voltage (from the on-board op amp) to be supplied to this reference input (high side). When it is unjumpered, an external high reference may be input to the pin closest to the DAC.

Table II - Control Table - Continued

NAME	DESCRIPTION
EFREF	When jumpered, the value of the REF H (Reference High) voltage from the on-board op amp is supplied to this reference input (high side). When it is unjumpered, an external high reference may be input to the pin closest to the DAC.
GHREF	Jumperering allows the value of the REF H (Reference High) voltage (from the on-board op amp) to be supplied to this reference input (high side). When it is unjumpered, an external high reference may be input to the pin closest to the DAC.
ABGND	When jumpered, the value of the REF L (Reference Low) voltage (from on-board op amp) is supplied to this reference input (low side). When it is unjumpered, an external low reference may be input to the pin closest to the DAC.
CDGND	When jumpered, the value of the REF L (Reference Low) voltage (from on-board op amp) is supplied to this reference input (low side). When it is unjumpered, an external low reference may be input to the pin closest to the DAC.
EFGND	When jumpered, the value of the REF L (Reference Low) voltage (from on-board op amp) is supplied to this reference input (low side). When it is unjumpered, an external low reference may be input to the pin closest to the DAC.
GHGND	When jumpered, the value of the REF L (Reference Low) voltage (from on-board op amp) is supplied to this reference input (low side). When it is unjumpered, an external low reference may be input to the pin closest to the DAC.
REF L	Jumperering this pin to AGND forces the reference input low at analog ground. When jumpered to the Reference Low position, the low reference takes on the value of the Reference Low adjust.
REF LOW ADJ	(R32) This potentiometer adjusts the value for the Reference Low from analog ground to one-half the value of the Reference High output. This may be supplied to the Reference Low inputs of the eight DACs
REF HIGH ADJ	(R34) This potentiometer adjusts the value for the Reference High from approximately +1.5 to +4.5 V.

OPERATIONAL DETAILS

This evaluation board was designed to be as flexible as possible for control of the eight DACs in the SPT5400. It was designed to operate just one DAC or all eight DACs in automatic sequence. To accomplish automatic sequencing through each DAC, a counter and a decoder were implemented on this evaluation board.

A description of the board when set to sequential eight DAC operation follows. (See the timing diagram as necessary.) The clock input supplies the clock for the counter. On the low half-cycle of the clock, the decoder output is enabled which allows for the active-low write strobe (this loads the first latch of the address pointed to by the counter) or enables the load for the respective address pointed to by the counter when the LSB of the counter is low or high respectively. The second half of the decoder is used to decode which load strobe is asserted. In the single address mode, the operation is the same except the address pointed to is fixed by the address select switch. Note that it takes two rising clock edges to complete a latched mode operation for either cycling through the eight DACs or a single DAC.

If the /WR (latch write signal) is forced low (jumpered to DGND), all the first latches are transparent when its associated address is asserted and stable. If any of the /LDXX (load DAC latch) is forced low, the second latch to the DAC pair is transparent. If a fixed voltage value out is required, at least one of the latches (write-latch or load-latch) must be made nontransparent (i.e., latch the data) at the appropriate data value input.

All control signals can be easily wired for external control. They include ADDRESS, /LDAB, /LDCD, /LDEF, /LDGH, /WR, /CLR, /PE and /CS.

Table III - Typical Operation Control

MODE	CLK RATE	ADD SEL	/PE	/WR	/CS	/CLR	/LDAB	/LDCD	/LDEF	/LDGH	DESCRIPTION
CLEAR	NA	NA	NA	NA	NA	LOW	NA	NA	NA	NA	All outputs at mid scale.
8-DAC FULL LATCH	16X	NA	OPEN	AUTO	PU	PU	AUTO	AUTO	AUTO	AUTO	DACs are loaded in sequence. Both latches are active (A - H).
8-DAC WRITE LATCH	16X	NA	OPEN	AUTO	PU	PU	PD	PD	PD	PD	DACs are loaded in sequence on the write strobe. The second latch is transparent.
8-DAC LOAD LATCH	16X	NA	OPEN	PD	PU	PU	AUTO	AUTO	AUTO	AUTO	DACs are loaded in sequence on their respective load strobe. When the address changes, data is in the write latch.
8-DAC TRANSA-RENT	16X	NA	OPEN	PD	PU	PU	PD	PD	PD	PD	DACs are loaded with the data present on data bus when the respective address is present.
ONE DAC FULL LATCH	2X	0 - 7 (i.e., A - H)	JUM-PER	AUTO	PU	PU	AUTO (if add is 0 or 1)	AUTO (if add. is 2 or 3)	AUTO (if add. is 4 or 5)	AUTO (if add. is 6 or 7)	The selected DAC is updated with full latch operation. The voltage is output after the second clock edge.
ONE DAC WRITE LATCH	2X	0 - 7 (i.e., A - H)	JUM-PER	AUTO	PU	PU	PD	PD	PD	PD	The selected DAC is updated with the write strobe. The voltage is output after the first clock edge.
ONE DAC LOAD LATCH	2X	0 - 7 (i.e., A - H)	JUM-PER	PD	PU	PU	AUTO (if add. is 0 or 1)	AUTO (if add. is 2 or 3)	AUTO (if add. is 4 or 5)	AUTO (if add. is 6 or 7)	The selected DAC is updated with the respective load strobe. The voltage is output after the second clock edge.
ONE DAC TRANSP-ARENT	2X	0 - 7 (i.e., A - H)	JUM-PER	PD	PU	PU	AUTO (if add. is 0 or 1)	AUTO(if add. is 2 or 3)	AUTO- (if add. is 4 or 5)	AUTO- (if add. is 6 or 7)	The selected DAC is updated with the address. The voltage is output after first clock edge. (Subsequent clocks are not required. The voltage output will change with data value change.)

NOTES:
PD (pull down), PU (pull up), AUTO (in auto load/write position). Clock X indicates the rate of the clock relative to the data update. For example, with a 2X clock, the data needs to be present for the first part of the write cycle, and it takes a second rising edge to complete the DAC load.

Figure 1 - Logic Control Circuit Diagram

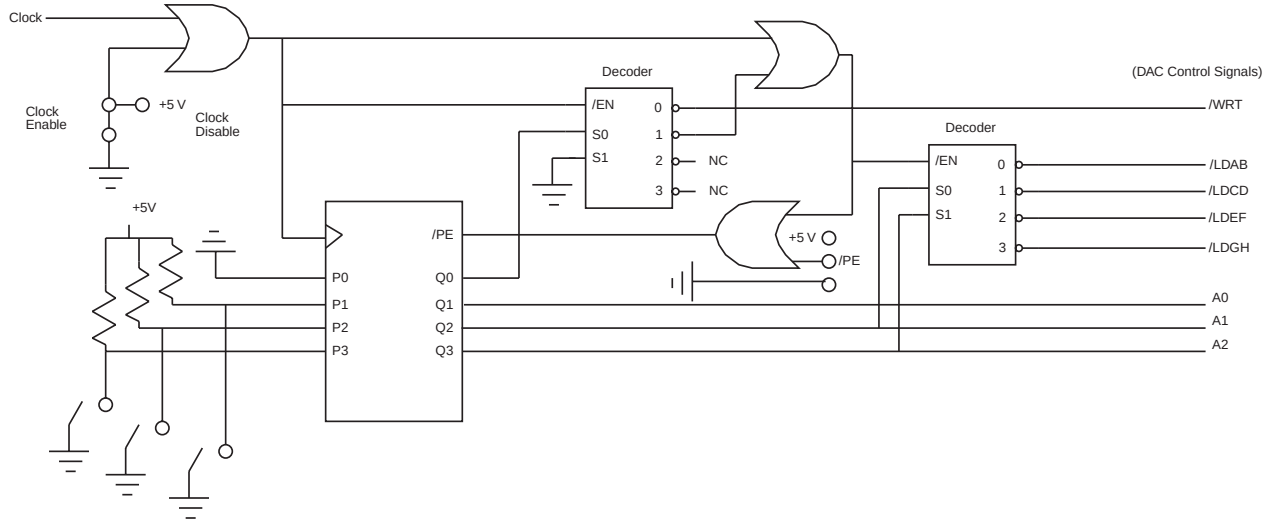


Figure 2 - Key Control Diagram

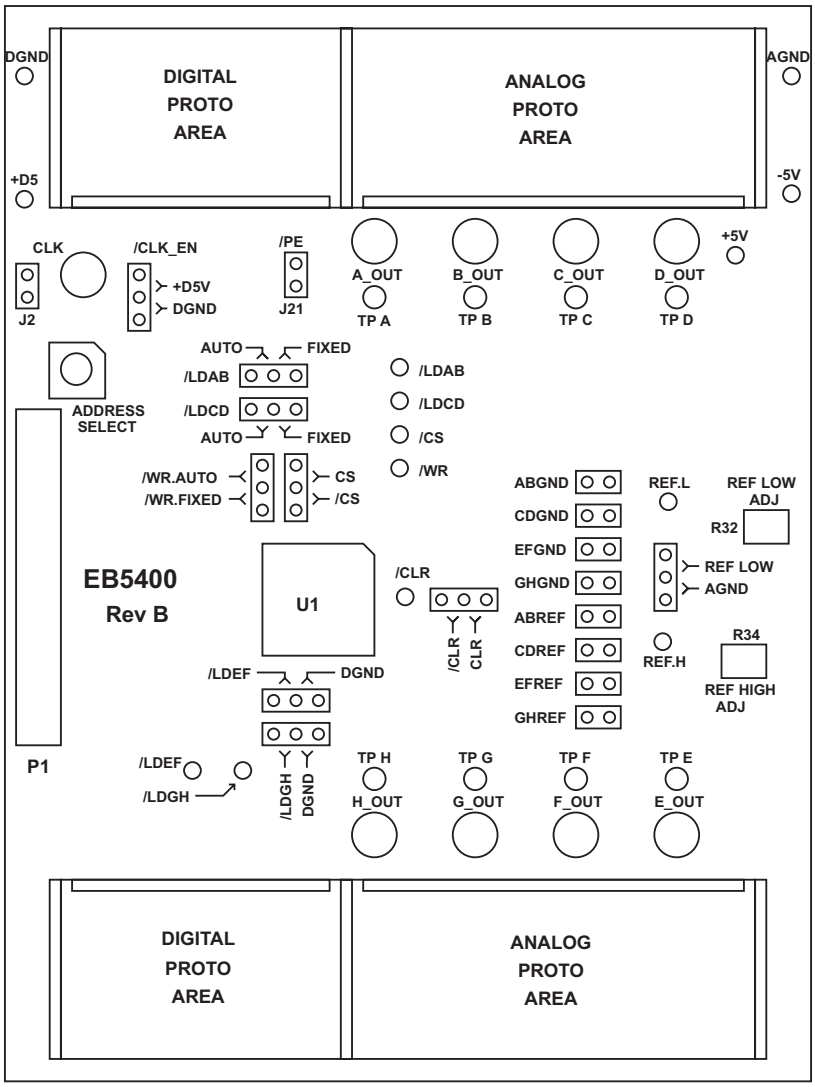
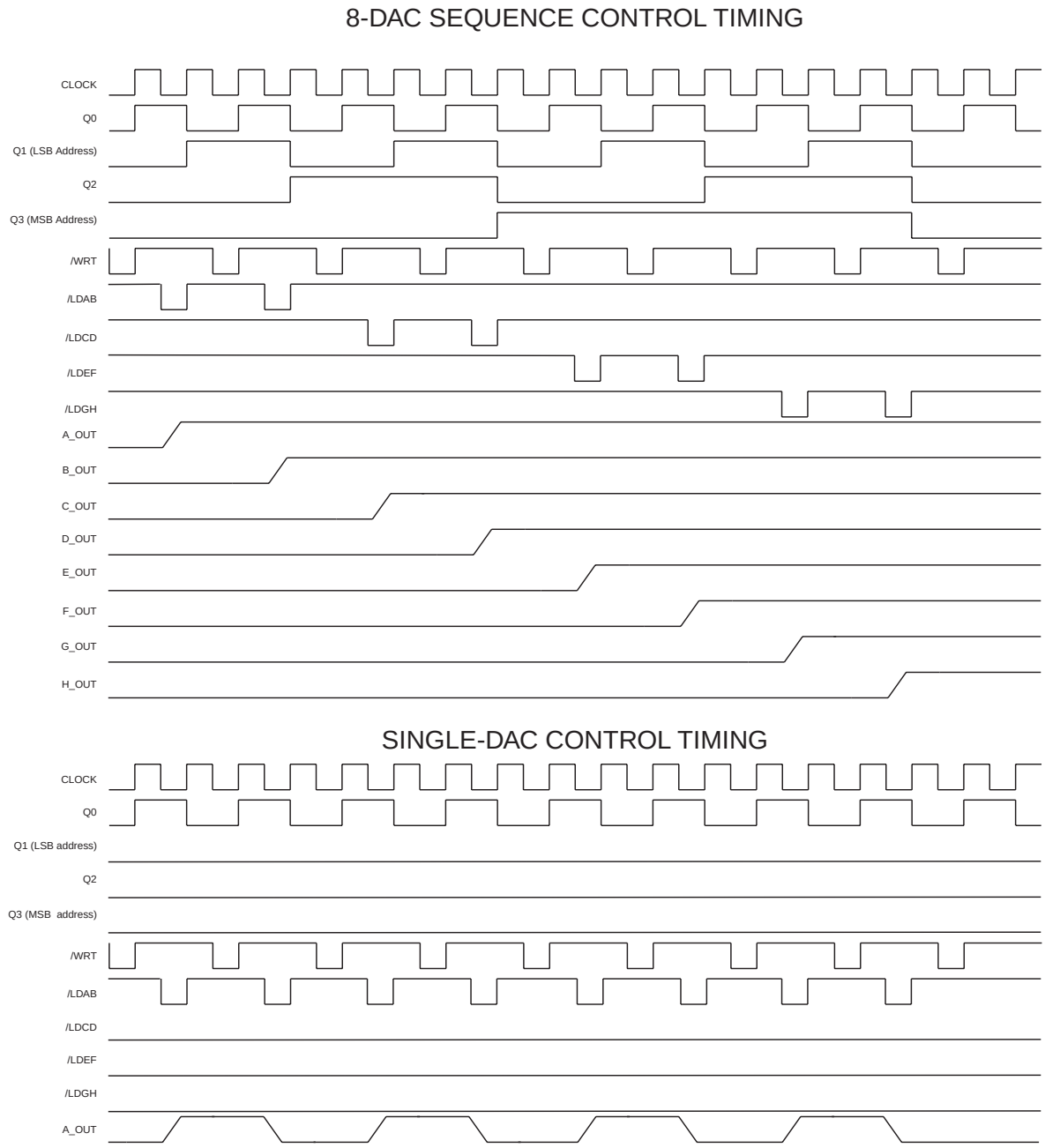


Figure 3 - Timing Diagram



NOTES:
1. Assume a 200 kHz clock.
2. The full timing diagram shows full latched operation for sequence of all eight DACs.
3. Assume output was negative full-scale and loaded with full scale high value.
4. Output voltage is relative in this diagram, and exact output values are a function of the reference voltage. (See the Reference section.)
5. The bottom diagram shows full latched operation for DAC A (address 0), with data input alternating between negative and positive full-scale.

CLOCK

A clock input is only required when operating the SPT5400 in its latched modes. If a latch mode is required, this design requires a clock that operates at two times the frequency of the data update rate. (See the timing diagram below.) The clock signal can be applied to the board via the J3 SMA connector or to the P1 (connector pin 1).

REFERENCE CIRCUIT

There are eight DACs in the SPT5400. The reference voltage is shared by groups of two; that is, DACs A-B share the same reference voltages as do C-D, E-F and G-H.

Operation of the reference voltage for this evaluation board is as follows. A stable reference voltage is provided by Z1 (1.2 V zener). This provides the reference voltage for the Reference High op amp. The Reference High voltage is supplied by one-half of U5 by adjusting the R34. This op amp is designed with a gain of four which provides a Reference High between +1.5 to +4.5 V. The output of the op amp is sent to jumpers ABREF through GHREF and to the other half of U5.

The other half of U5 is used to provide a Low Reference voltage. It is designed as a voltage follower. The output voltage may be adjusted between AGND and one-half of the Reference High. This Reference Low voltage can provide for a symmetrical bipolar up to unipolar operation and all levels in between.

The following are tips for other reference design concepts:

- Use a star configuration if all pins are using a common reference and/or ground reference.
- The analog ground reference input may operate between the supply rails (V_{DD} to V_{SS}). However, the output is limited to the V_{SS} supply less 0.5 V from the rail. The Reference High input must be a more positive level than the AGND input.
- Separate reference buffering may be applied. Use op amps that can drive capacitive loads. Sense the reference voltage at the pin of the SPT5400 for accurate reference voltages.
- Input reference resistance for both Reference High and AGND input need to be considered when all input references are being driven from a common source (parallel loads). Refer to the minimum reference resistance information in the data sheet.
- The output of DAC may be used for a reference voltage to other DAC pairs. (Do not use the output as a self-reference.)

Refer to the Analog Output section of this document for attainable output voltage values with the SPT5400.

MULTIPLYING OPERATION

The SPT5400 can be used for multiplying in a two-quadrant application. When using AC signals on the reference inputs, do not use filter capacitors. Limit the amplitude of the input Reference High and AGND inputs to the level the output can achieve. Refer to the Analog Output section to determine the level the reference input signals can attain. The input capacitance of the reference pins is not sufficient to serve as a low-pass filter in the frequency range in which the SPT5400 multiplies. To achieve near 13-bit results in multiplying applications, the input reference voltage must not slew at a rate that causes the output to slew faster than the rate specified in the data sheet.

ANALOG OUTPUT

The output can operate in bipolar, unipolar or a level-shifted bipolar operation. Due to a common reference to a pair of DACs, there will be a slight perturbation from one to the other output when one DAC is updated.

Always refer to the latest data sheet for this part when designing for a specific output voltage requirement.

Table IV - Reference Voltage Settings vs. Output Voltage

Parameter	Description	Output Voltage Value
Volts per LSB (V/LSB)	Voltage per Bit	2*(HREF - LREF)/8192
Positive Full Scale	Full Scale (1FFFh) High	[HREF*4095 + LREF]/4096 or HREF -1 V/LSB
Negative Full Scale	Full Scale (0000h) Low	2*LREF - HREF
Mid Scale	Middle Scale (1000h) MID	LREF
Output vs. Digital Input	D (Digital Input Pattern) D=0 to 8191	[HREF*(D-4096) + LREF*(8192-D)]/4096

NOTES:

1. Bipolar Operation: For symmetrical bipolar operation, set the Reference High to maximum positive full scale and Reference Low to analog ground.
2. Unipolar Operation: For positive unipolar operation, set the Reference High to maximum positive full scale value and Reference Low to one-half of the high reference value. For negative unipolar operation, set Reference Low to negative full scale value and Reference High to zero volts.
3. Custom Operation: Set Reference High to the positive full scale value and Reference Low to the following equation: LREF = (HREF - |Vlow|)/2 (where Vlow is the maximum negative value).

LAYOUT

Fairchild carefully considered the layout of this evaluation board to ensure maximum performance of the part. It was designed to aid the user in developing similar designs and layout aspects. Some highlights of the design are as follows:

- Stable reference voltage designs
- Digital pull-down resistors to protect input to the SPT5400
- Series resistors for transient suppression
- Generous decoupling and filtering on all power supply and analog input signals
- Split power and ground planes

TEST POINTS

There are several test points on key signals. They are described in the table below.

Table V - Key Signal Test Points

TEST	DESCRIPTION
X_OUT	Analog output signal from the respective DAC. Accommodates a 5 mm probe tip.
Ref. H	Reference High, i.e., the reference voltage sourced by the on-board reference buffer op amp.
/WR	Monitors the active-low write signal pin of the DAC.
/CLR	Monitors the active-low clear signal pin of the DAC.
Ref. L	Reference Low, i.e., the reference voltage sourced by the on-board reference buffer op amp.
/LDXX	Monitors the respective active-low load pins (AB - GH).
/CS	Monitors the active-low chip select pin of the DAC.
DGND, AGND, +D5 V, +A5 V, -A5 V	Test or supply points for power and ground.

PROTOTYPE AREAS

Prototype areas for digital and analog circuits are provided to meet your individual requirements. To use the signal out of the DACs in the prototype area, jumper the signal to the prototype area. Power is provided as indicated on the silk screen.

INITIAL SETUP AND OPERATIONAL CHECK

Before connecting to the P1 connector, verify that all power sources, including logic, are disabled,

Perform the following steps for initial set up and functional verification.

1. Set the power supplies to within ± 100 mV of their nominal value. If using two separate +5V supplies remove FB2.
2. Connect the power supplies to either their respective test point input or to the correct pin input on P1. (Refer to the pin connection table.)
3. Ensure that the logic input signals (including the clock signal) are at zero volts and are powered off.
4. Connect the customer-provided P1 connector.
5. Depending on your clock source, do the following:
   P1-pin 1 input: Install R37 and remove R14 J3-(SMA clock input). Remove R37 and install R14 (50 ohm).
6. Set the clock input to 1 kHz, square wave TTL level. Disable before connecting to the EB5400.
7. Set all controls and jumpers indicated in the table as follows: (Refer to key table diagram.)

Table VI - Control/Jumper Positions

Control/ Jumper	Position	Control/ Jumper	Position
J31 (CLK EN)	DGND	Address Select	Don't Care
J21 (/PE)	Unjumpered	/WR	Auto
/CS	CS	/LDAB	Auto
/LDCD	Auto	/LDEF	Auto
/LDGH	Auto	/CLR	CLR
Ref Low	AGND	R34 (Ref High Adj)	Full CW Position
XXGND	Jumper All	REFXX	Jumper All

8. Turn on the power supplies.
9. Set Reference High to +4.096 V by adjusting R34.
10. Set the clock to enable. Set the input data pattern to 0000 hex (minimum input) at logic inputs.
11. Monitor the output of each analog signal (A_OUT through H_OUT). Verify that the output levels are at -4.096 V ± data sheet value for zero code error.
12. Set the input data pattern to 1FFF hex (maximum input) and monitor the analog outputs. Verify that the output is +4.095 V ± data sheet value for gain error.
13. Jumper the /CLR position. Verify that all outputs go to mid scale. (Include the calculated mid scale offset based on the zero and gain values obtained in steps 11 and 12.)
14. This concludes initial functional operation. For other desired operation, ensure the data update relative to the respective clock meets setup and hold times.

Figure 4 - Detailed Schematic, Rev. B Board

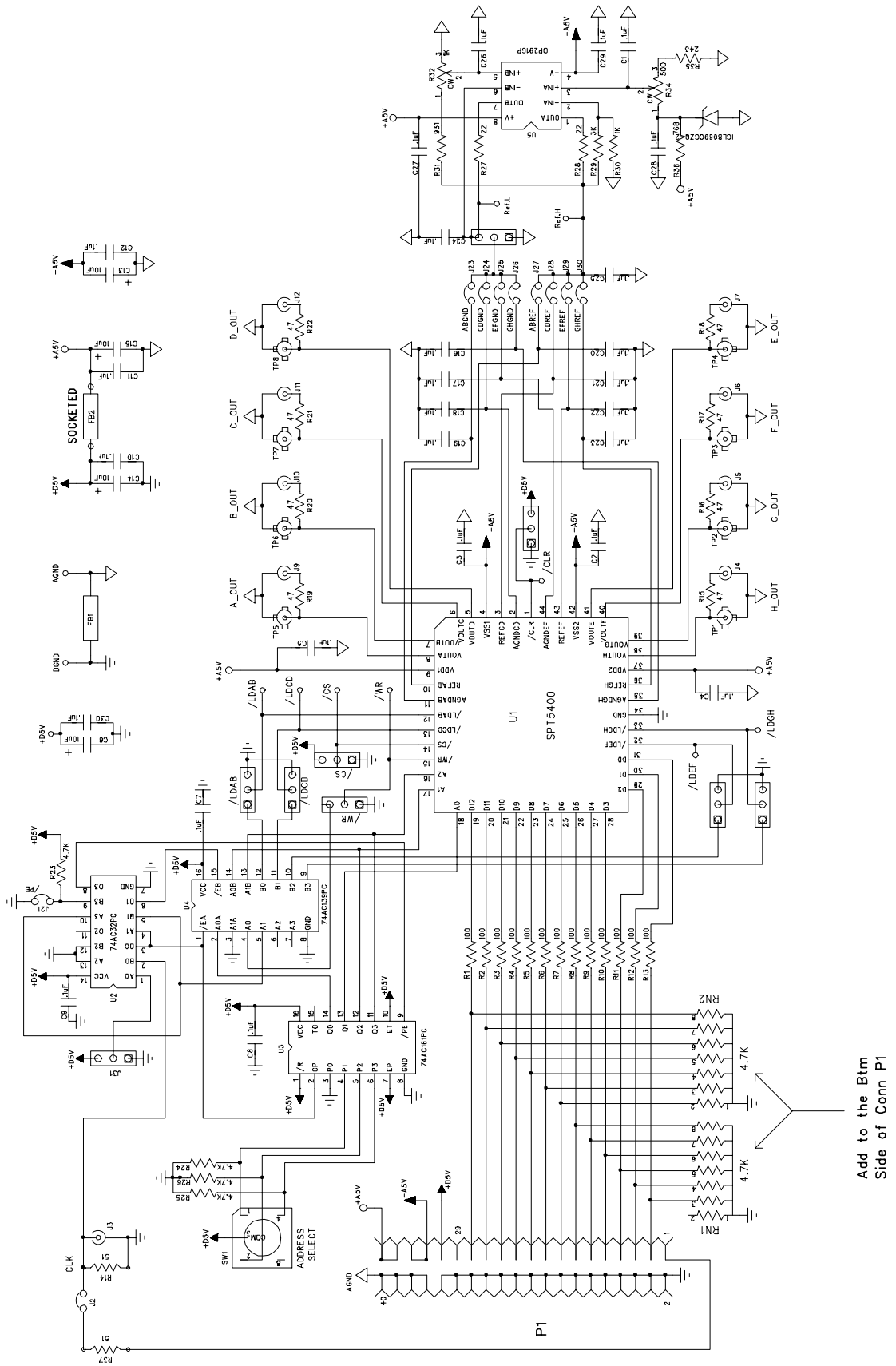


Table VI - Bill of Materials

No.	Reference	Description	Part Number	Qty	Vendor
1	C1-5,7-12,16-30	ECU-V1H104KB	.1 µF Chip Cap	26	Panasonic/Any
2	C6,13-15	ECS-TICX106R	10 µF Tantalum Chip Cap	4	Panasonic/Any
3	D1	ICL8069CCZQ-2	1.2 V Ref. Zener	1	Maxim
4	FB1,2	EXC-ELSA35	Ferrite Bead	2	Panasonic
5	J1	PZC36DBAN	72-Pin Horiz Male Conn [Trim to 40-Pin]	1	Sullins
6	J2,21,23-30	PZC36SAAN	Jumper, 2 Pin [Trim from 36-Pin]	10	Sullins
7	J3-7,9-12	901-144-8	SMA Coax Connector	9	Amphenol
8	J8,13,16-20,22,31	PZC36SAAN	Jumper, 3 Pin [Trim from 36 Pin]	10	Sullins
9	R1-13	ERJ-8ENF1000	100 Ohm Chip Resistor	13	Panasonic/Any
10	R14,37	51 MF	51 Ohm 1/4 W 1% Axial [Socketed]	2	Yageo /Any
11	R15-22	ERJ-8ENF47R5	47.5 Ohm Chip Resistor	8	Panasonic/Any
12	R23-26	ERJ-8ENF4701	4.7kΩ Chip Resistor	4	Panasonic/Any
13	R27,28	ERJ-8ENF22R1	22.1 Ohm Chip Resistor	2	Panasonic/Any
14	R29	ERJ-8ENF3011	3.01 kΩ Chip Resistor	1	Panasonic/Any
15	R30	ERJ-8ENF1001	1.0 kΩ Chip Resistor	1	Panasonic/Any
16	R31	ERJ-8ENF9310	931 Ohm Chip Resistor	1	Panasonic/Any
17	R32	3266W-1-102	1 kΩ Variable Resistor (Pot)	1	Bourns
18	R34	3266W-1-501	500 Ohm Variable Resistor (Pot)	1	Bourns
19	R35	ERJ-8ENF2430	243 Ohm Chip Resistor	1	Panasonic/Any
20	R36	ERJ-8ENF7680	768 Ohm Chip Resistor	1	Panasonic/Any
21	RN1,2	770-81-R4.7K	8 Pin, 7 Res SIP Network	2	CTS / Any
22	SW1	A6A-16R	Rotary DIP Switch	1	Omron
23	TP9-20	40F6045	Solder Terminal	12	NEWARK
24	U1	SPT5400	13-Bit Octal DAC	1	Fairchild
25	U2	74AC32PC	Quad 2-Input OR Gate	1	Fairchild/Any
26	U3	74AC161PC	Synchronous Counter	1	Fairchild/Any
27	U4	74AC139PC	Dual 1-of-4 Decoder	1	Fairchild/Any
28	U5	OP291GP	Dual R-R Op Amp	1	Analog Devices
29	N/A	1902EK-ND	1" Nylon Spacer	4	DIGI-KEY
30	N/A	H143-ND	4-40 Pan-head Screw	4	DIGI-KEY
31	N/A	ED5044-ND	Pin Receptacle [For socketed resistors]	2	DIGI-KEY
32	N/A	929955-06	Shunt for Jumpers	19	3M (DIGI-KEY)
33	EB5400	Rev B	Evaluation Board	1	SAS Circuits

Figure 3 - Component Side

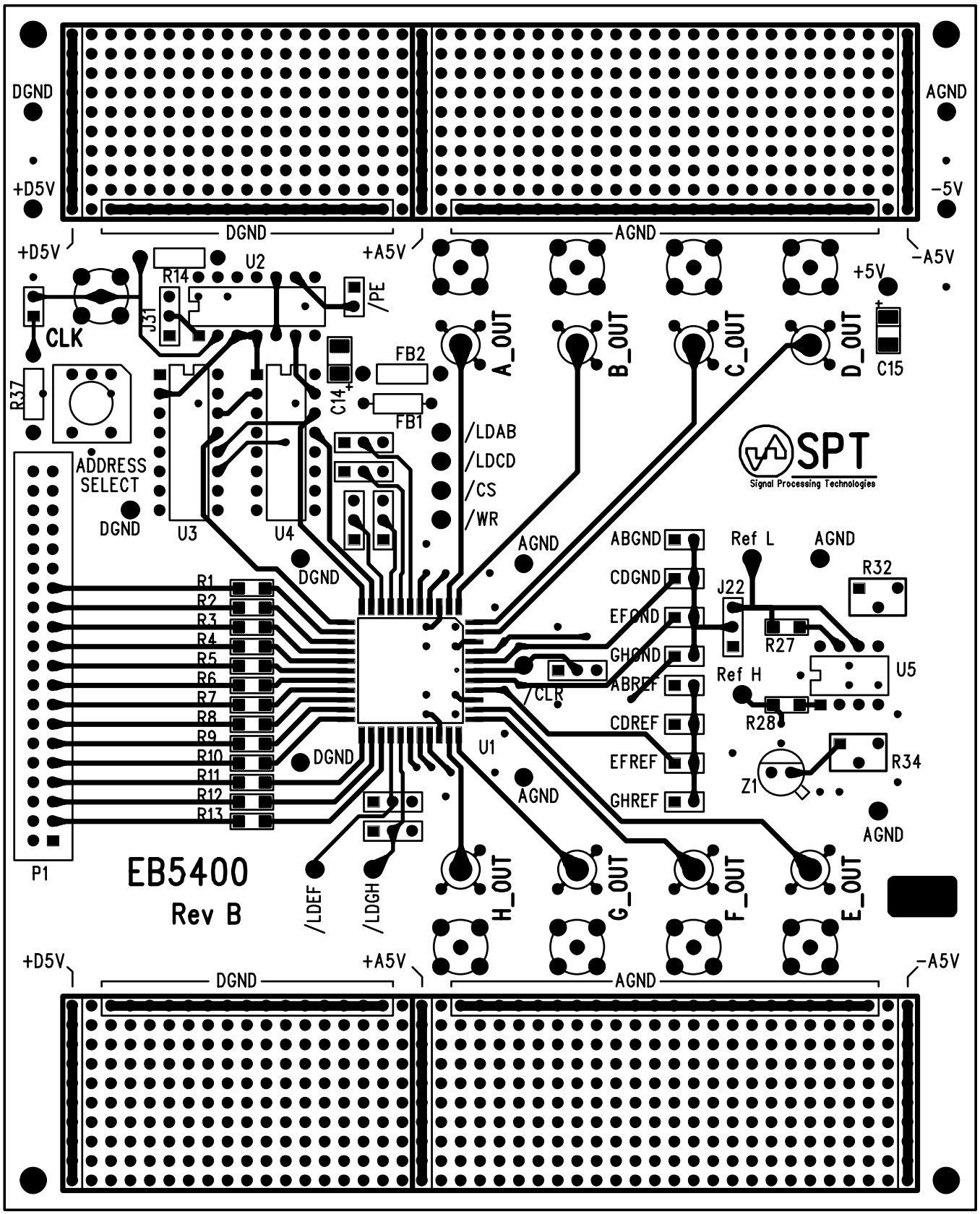


Figure 4 - Ground Layer

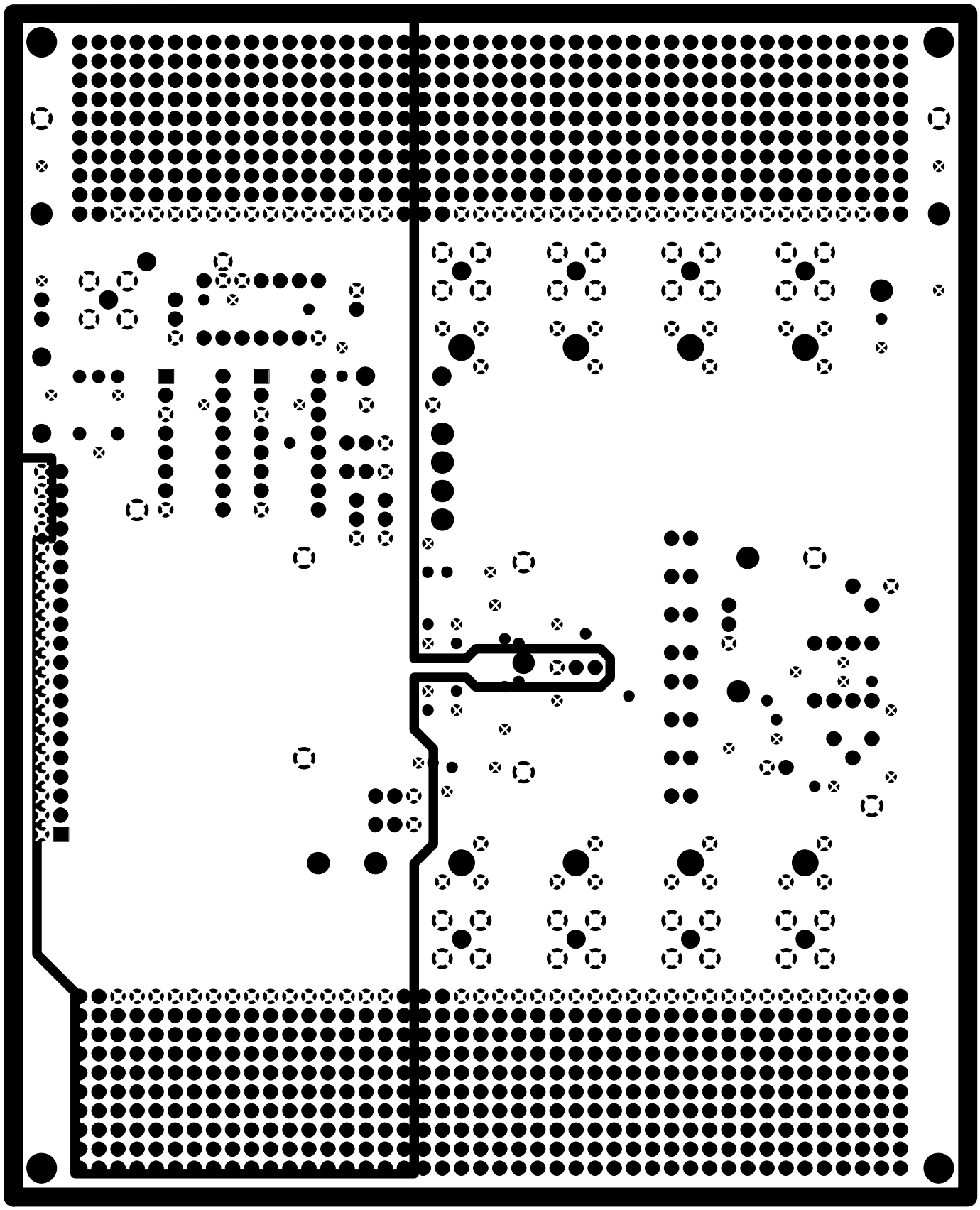


Figure 5 - Power Layer

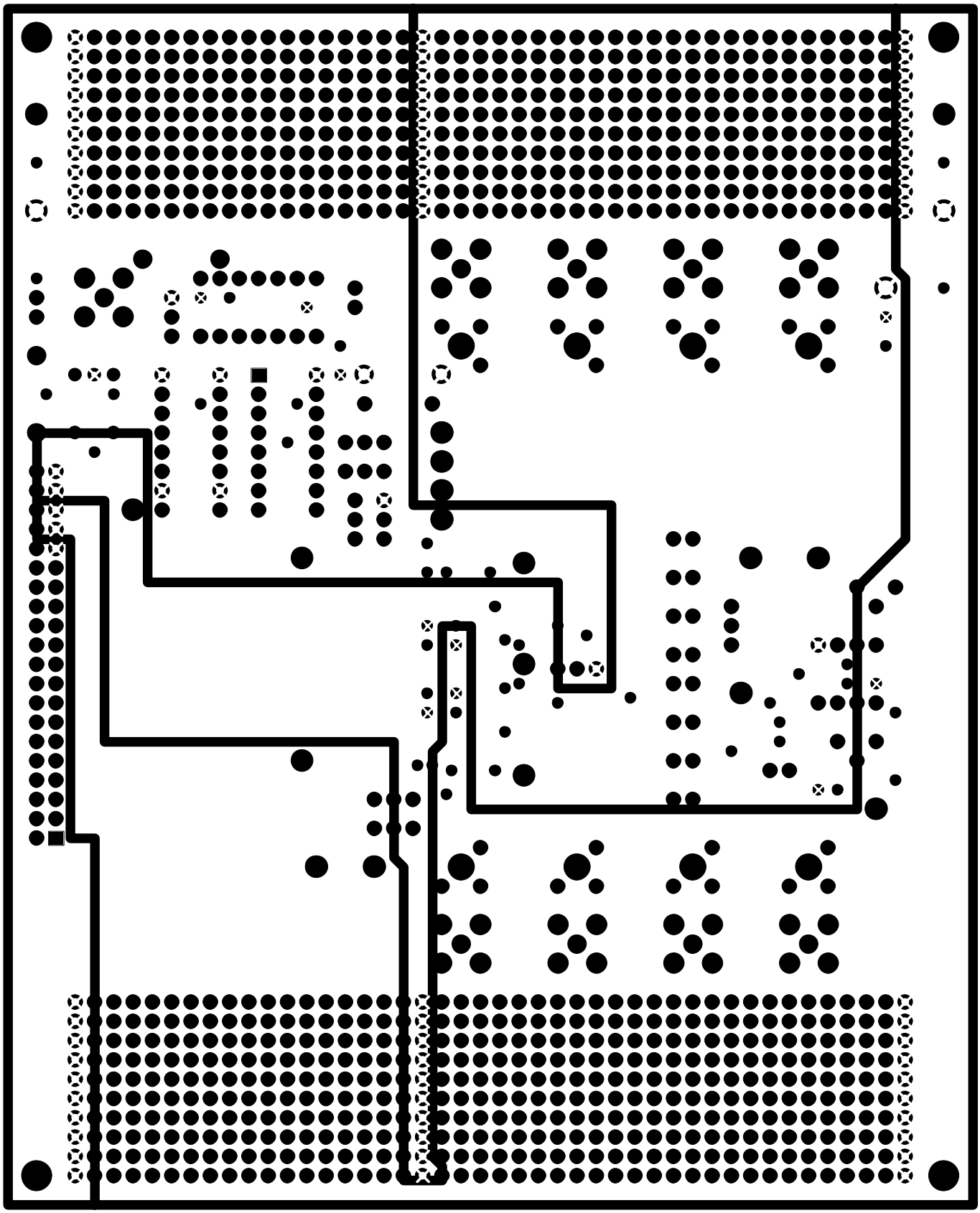
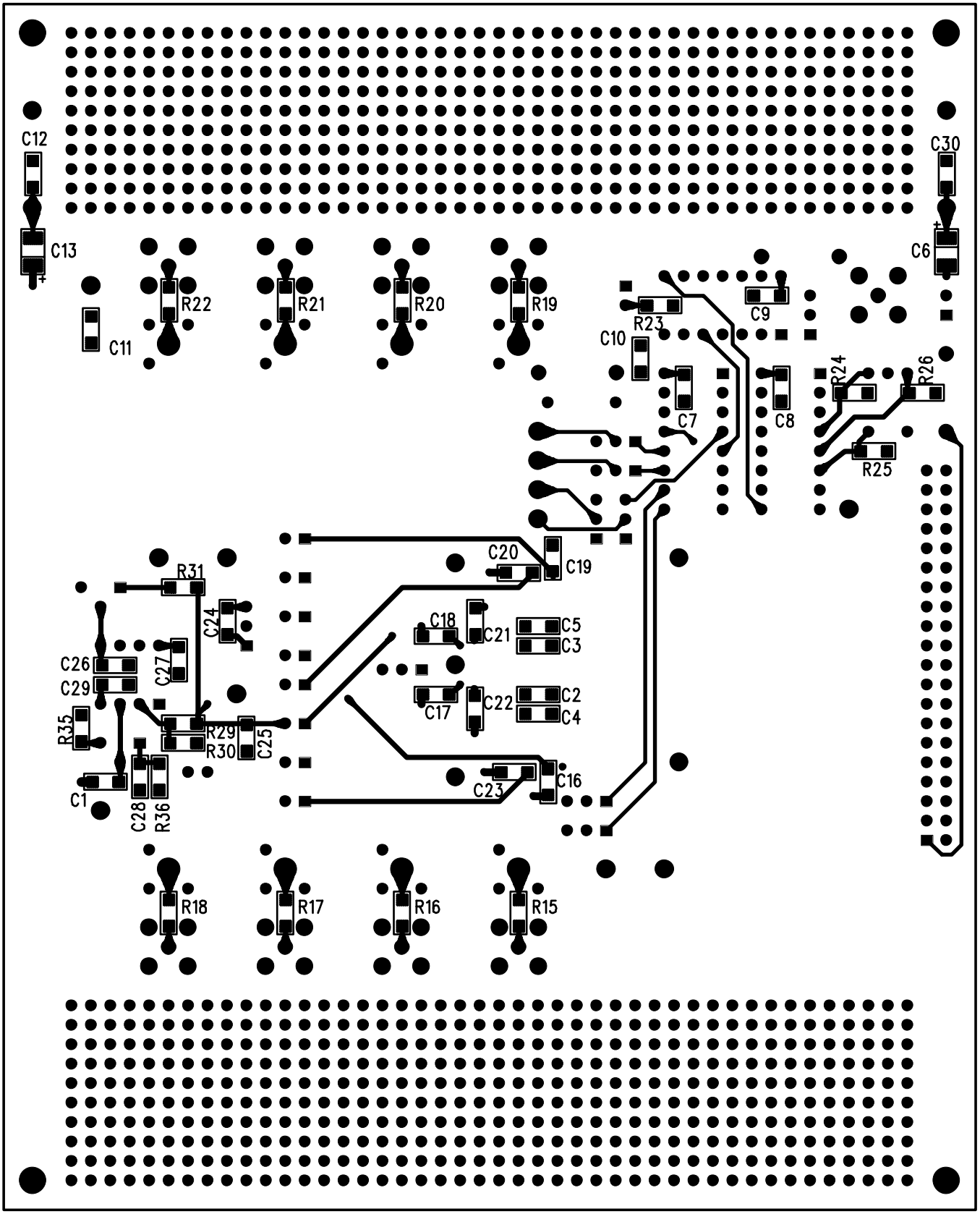


Figure 6 - Solder Side



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